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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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JOSEPH S. TRIPOLI
THOMSON MULTIMEDIA LICENSING INC.
2 INDEPENDENCE WAY
P.O. BOX 5312
PRINCETON, NJ 08543-5312

EXAMINER	
NATNAEL, PAULOS M	

ART UNIT	PAPER NUMBER
2614	2

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,484	WILLIS, DONALD HENRY	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1-13** rejected under 35 U.S.C. 103(a) as being unpatentable over Chambers et al., U.S. Patent No. 6,437,828 in view of Adams et al, U.S. Pat. No. 6,380,978.

Considering claim **1**, Chambers et al discloses the following claimed subject matter, note;

a) the claimed method of receiving the standard definition television signal to provide a received signal, is met by the A/V sub-system 102, figs.1-4, which is capable of receiving several signals including from TV, VCR, DSS, and FM. (see also col. 5, lines 40-44)

b) the claimed method of sampling the received signal to provide a sampled digital video signal, is met by the A/D converter 310 (fig.3) in the path 300 within the A/V subsystem 102.

c) deinterlacing the sampled digital video signal to provide a progressive line signal, is met by the deinterlacer 212, fig.3;

d) the claimed method of doubling the progressive line signal to provide a predetermined number of active lines of video in a frame, is met by the scaler 408, which further scales the video signal in the PC 104 to output a scaled, deinterlaced video signal to the progressive display monitor 110, fig. 3; (see also Abstract, wherein Chambers teaches that the "combination of the line doubler [402] and the scaler [408] is made to function as a line quadrupler.") [emphasis added by examiner]

Except for;

e) displaying the predetermined number of active lines of video on the high definition matrix display in a shortened vertical interval.

Regarding e), Chambers et al. disclose high-resolution and progressive scan monitor 110. Chambers does not specifically disclose high definition matrix display. However, such displays are well known in the television art. In that regard, Adams et al for example discloses a digital video system and method comprising an LCD display 36 (fig.3), and suggests that active or passive matrix models may be utilized. (Adams, col. 7, lines 36-45) Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Chambers et al. by providing the LCD display of Adams et al. so that the high resolution, progressive-scanned or converted

signal would be properly displayed according to a desired high resolution and progressive scan displaying the deinterlaced and scaled (i.e., quadrupled) signal.

Considering claim **2**, the method of claim 1, where the method further comprises the step of storing the progressive line signal into a memory before the step of doubling, is met by EDO 412, fig.4, which is used to store the received data from the AV 102 and then read from it to display window 410. (see col. 6, lines 1-7)

Considering claim **3**, the method of claim 1, wherein the step of doubling comprises the step of reading each line of the progressive line signal twice from the memory to produce a standard 960p signal, wherein the progressive line signal is a 480p signal, is met by the output signal 1480X960, which is double the input signal 720X480 (fig.4) and by the disclosure that "... Graphics board 404 supplies video output data in a 1440.times.960 format (960 lines of 1440 pixels) de-interlaced or 720.times.960 interlaced...Interlaced output reduces required bandwidth. A simple manner to implement the interlaced output is to shift either the odd or the even fields by a half a single line, thus displaying the same field twice. This may introduce some line flicker, but this is acceptably little because of the now finer line structure." (col. 6, lines 8-17)

Considering claim **4**, the method of claim 2, wherein the method further comprises the step of reading each line of the progressive line signal twice from the memory at a

speed fast enough to produce the doubling of each line of the progressive line signal in the frame and to transmit the frame to the display in a shorter interval than was used to write the progressive line signal to the memory.

Regarding claim 4, Chambers et al., as shown in claim 3, discloses a doubled 1380X960 output signal (fig.4). Chambers also teaches that the combination of the doubler and scaler 408 functions as a line quadrupler. (see Abstract) Chambers does not specify the process of the doubler or the scaler. Nevertheless, the Examiner takes Official Notice here in that the method of reading lines of video data twice as fast than the speed of writing the data lines into a memory is notoriously well-known in the art, and therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Chambers by providing a memory in place of the scaler 408 to read the video signal at higher speed than it was written, so that the circuit is made compact by using only one memory instead of the memory EDO 412 and the scaler 408.

Considering claim **5**, the method of claim 4, wherein the shorter, interval compensates for the transmission of black lines transmitted at the top and bottom of the display.

Regarding claim 5, Chambers et al doesn't specifically disclose black lines at the top and bottom of the display. However, the Examiner is taking Official Notice here in that such black lines, in the so-called letter-box format, is notoriously well-known in the art, and therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Chambers by providing the letter-box

format in order to make the system of Chambers et al more flexible and display different types of display formats.

Considering claim **6**, the method of claim 1, wherein the method further comprises the steps of writing the signal corresponding to the predetermined number of active lines of video into a memory and reading out the predetermined number of active lines of video from the memory in a shorter time interval than was used to write the signal corresponding to the predetermined number of active lines of video into the memory.

Regarding claim 6, see rejection of claim 4.

Considering claim **7**,

a) wherein the signal corresponding to the predetermined number of active lines is a 960p frame which is read out of the memory;

Regarding a), see rejection of claim 3.

b) the claimed, transmitted to the display in approximately 88% of a vertical period.

As for b), Chambers et al does not specify any such number, however, it would be obvious matter of design choice to choose a particular speed at which the data is transmitted to the display or read from or written into memory, since the applicant has not disclosed that transmitting at 88% of the vertical period solves any stated problem or is for any particular purpose and it appears that any similar number, 90%, 91% or 87%, for that matter, would perform equally well.

Considering claim **8**, Chambers discloses the following claimed subject matter, note;

a) receiving the standard definition television signal to provide a received a signal, is met by the A/V sub-system 102 (figs.1 and 4), which is capable of receiving several signals including TV, VCR, DSS, and FM signals. (see also col. 5, lines 40-44)

b) sampling the received signal to provide a sampled digital video signal, is met by A/D converter 310 (fig.3) in the path 300 within the A/V subsystem 102.

c) deinterlacing the sampled digital video signal to provide a progressive line signal, is met by the deinterlacer 212, fig.3;

d) doubling the progressive line signal to provide a predetermined number of active lines of video in a frame, is met by the scaler 408, which further scales the video signal in the PC 104 to output a scaled, deinterlaced video signal to the progressive display monitor 110, fig. 3; (see also Abstract, wherein Chambers teaches that the "combination of the line doubler [402] and the scaler [408] is made to function as a line quadrupler.") [emphasis added]

e) storing the frame containing the predetermined number of active lines in a memory, is met by EDO 412, fig.4;

Except for;

f) reading the frame from memory and transmitting it to the high definition matrix display in a shortened vertical interval.

Regarding f), see rejection of claim 1(e) and claim 4.

Considering claim **9**, the method of claim 8, wherein the shortened vertical interval is approximately 88% of a vertical interval.

See rejection of claim 7(b).

Considering claim **10**, the method of claim 8, wherein the step of doubling comprises the step of repeating each line of the progressive line signal to produce a standard 960p signal, wherein the progressive line signal is a 480p signal.

See rejection of claim 1(c) and claim 3.

Considering claim **11**, the method of claim 8, wherein step of storing the frame, comprises the step of storing a 960p signal into the memory, is met by the disclosure that the "content of memory 412 represents the content of window 410" (col. 6, lines 5-7) which means the memory 412 stores the output data 1480X960, fig.4. [Note, the fig. 4 shows 1480X360 which is clearly a typo error. It should have been 1480X960, double 720X480 input signal)

Considering claim **12**, the method of claim 8, wherein the shorter interval compensates for the transmission of black lines transmitted at the top and bottom of the display.

Regarding claim 12, see rejection of claim 5.

Considering claim **13**, the method of claim 8, wherein the signal corresponding to the predetermined number of active lines is a 960p frame which is read out of the memory and transmitted to the display in approximately 88% of a vertical interval.

Regarding claim **13**, see rejection of claim 7.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Faroudja et al., U.S. Pat. No. 6,222,589 discloses displaying video on high-resolution computer-type monitors substantially without motion discontinuities.

Callway et al., U.S. Pat. No. 6,680,752 discloses method and apparatus for deinterlacing video.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
April 13, 2004

PAULOS M. NATNAEL
PATENT EXAMINER